

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.

Application No. Not yet assigned

Filed: February 17, 2004

Confirmation No. --

For: METHOD FOR SYNTHESIZING LINEAR
FINITE STATE MACHINES

Examiner: --

Art Unit: --

Attorney Reference No. 1011-67627

MAIL STOP PATENT APPLICATION
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
FOR CONTINUING APPLICATIONS

Listed on the accompanying form PTO-1449 are several English-language documents. Applicants respectfully request that such documents be listed as references cited on the issued patent.

The present application relies upon U.S. Patent Application No. 10/346,699, filed January 16, 2003, which is a continuation of U.S. Application No. 09/957,701, filed September 18, 2001, which is a continuation of U.S. Application No. 09/620,023, filed July 20, 2000, which claims the benefit of U.S. Provisional Application No. 60/167,455, filed November 23, 1999, for an earlier filing date under 35 U.S.C. § 120. Furthermore, documents listed on the accompanying form PTO-1449 were disclosed to or cited by the Patent Office in the earlier U.S. application.

Copies of the documents listed on the accompanying form PTO-1449 that were cited by

or submitted to the Patent Office in the earlier application need not be sent to the Patent Office pursuant to 37 C.F.R. § 1.98. However, applicants will furnish the Patent Office with such copies upon request.

The filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By 

Patrick M. Bible
Registration No. 44,423

One World Trade Center, Suite 1600
121 S.W. Salmon Street
Portland, Oregon 97204
Telephone: (503) 226-7391
Facsimile: (503) 228-9446

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Attorney Docket Number	1011-67627
	Application Number	Not yet assigned
	Filing Date	February 17, 2004
	First Named Inventor	Rajski
	Art Unit	--
	Examiner Name	--

U.S. PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Number	Date	Name
		3,614,400	Oct-71	Farnett
		3,700,869	Oct-72	Low et al.
		4,503,537	Mar-85	McAnney
		4,513,418	Apr-85	Bardell, Jr., et al.
		4,602,210	7/1986	Fasang et al.
		4,687,988	Aug-87	Eichelberger et al.
		4,754,215	Jun-98	Kawai
		4,785,410	Nov-88	Hamatsu et al.
		4,801,870	Jan-89	Eichelberger et al.
		4,860,236	Aug-89	McLeod et al.
		4,959,832	Sep-90	Bardell, Jr.
		4,974,184	Nov-98	Avra
		5,090,035	Feb-92	Murase
		5,138,619	Aug-92	Fasang et al.
		5,173,906	Dec-92	Dreibelbis et al.
		5,268,949	Dec-93	Watanabe

EXAMINER SIGNATURE:	DATE CONSIDERED:
<p>* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Attorney Docket Number	1011-67627
	Application Number	Not yet assigned
	Filing Date	February 17, 2004
	First Named Inventor	Rajski
	Art Unit	--
	Examiner Name	--

U.S. PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Number	Date	Name
		5,301,199	Apr-94	Ikenaga et al.
		5,325,367	Jun-94	Dekker et al.
		5,369,648	Nov-94	Nelson
		5,394,405	Feb-95	Savir
		5,412,665	May-95	Gruodis et al.
		5,414,716	May-95	Bershteyn
		5,446,683	Aug-95	Mullen et al.
		5,450,414	Sep-95	Lin
		5,574,733	Nov-96	Kim
		5,586,125	Dec-96	Warner
		5,592,493	Jan-97	Crouch et al.
		5,612,963	Mar-97	Koenemann et al.
		5,631,913	May-97	Maeda
		5,694,402	Dec-97	Butler et al.
		5,719,913	Feb-98	Maeno
		5,748,497	May-98	Scott et al.
		5,790,562	Aug-98	Murray et al.

EXAMINER
SIGNATURE:

DATE
CONSIDERED:

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Attorney Docket Number	1011-67627
	Application Number	Not yet assigned
	Filing Date	February 17, 2004
	First Named Inventor	Rajski
	Art Unit	--
	Examiner Name	--

U.S. PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Number	Date	Name
		5,790,626	Aug-98	Johnson et al.
		5,831,992	Nov-98	Wu
		5,899,961	May-99	Sundermann
		5,905,986	May-99	Rohrbaugh et al.
		5,974,433	Oct-99	Currie
		5,991,898	Nov-99	Rajski et al.
		6,072,823	June-00	Takakusaki
		6,141,669	Oct-00	Carleton
		6,158,032	Dec-00	Currier et al.
		6,300,885	Oct-01	Davenport et al.
		6,327,687	12-01	Rajski et al.
		6,385,750	May-02	Kapur et al.
		09/713,662	07/20/2000	Rajski et al.
		09/713,664	11/15/2000	Rajski et al.

FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Number	Date	Country
		WO 01/38889 A1	31 May 2001	PCT

EXAMINER
SIGNATURE:

DATE
CONSIDERED:

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Attorney Docket Number	1011-67627	
		Application Number	Not yet assigned	
		Filing Date	February 17, 2004	
		First Named Inventor	Rajski	
		Art Unit	--	
		Examiner Name	--	
FOREIGN PATENT DOCUMENTS				
Examiner's Initials*	Cite No. (optional)	Number	Date	Country
		WO 01/39254 A3	31 May 2001	PCT
Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS		
		Mano, M. Morris, "Computer System Architecture," 2 nd Edition, Prentice-Hall, Inc., New Jersey, 1982, pp. ii and 50-54.		
		Bershteyn, Michael, "Calculation of Multiple Sets of Weights for Weighted Random Testing," International Test Conference 1993, Paper 45.3, pp. 1031-1040.		
		Zacharia, N., "Decompression of Test Data Using Variable-Length Seed LFSRs," IEEE 1995, 426-432.		
		P.H. Bardell, "Design Considerations for Parallel Pseudorandom Pattern Generators", Journal of Electronic Testing: Theory and Applications, pp. 73-87 (1990)		
		I. Hamzaoglu, J. Patel, "Reducing Test Application Time for Full Scan Embedded Cores," Center for Reliable & High-Performance Computing, University of Illinois, Urbana, IL., 1999 IEEE, pp. 260-267.		
		S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman, B. Courtois, "Built-in Test for Circuits With Scan Based on Reseeding of Multiple Polynomial Linear Feedback Shift Registers", <i>IEEE Trans. On Computers</i> , vol. C-44, pp. 223-233, 1995.		
		S. Hellebrand, B. Reeb, S. Tarnick, H-J Wunderlich, "Pattern Generation for a Deterministic BIST Scheme", pp. 88-94 1995 IEEE		
		B. Koenemann c/o IBM Corp. , B56/901, "LFSR-Coded Test Patterns for Scan Designs", <i>Proceedings of European Test Conference</i> , pp. 237-242, 1991.		
		J. Rajski, J. Tyszer, N. Zacharia, "Decompression of Test Data Using Variable-Length Seed LFSRs", Microelectronics and Computer Systems Laboratory, McGill University, Montreal, Canada, 1995 IEEE, pp. 426-433		

EXAMINER SIGNATURE:	DATE CONSIDERED:
* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Attorney Docket Number	1011-67627
		Application Number	Not yet assigned
		Filing Date	February 17, 2004
		First Named Inventor	Rajski
		Art Unit	--
		Examiner Name	--
Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS	
		J. Rajski, J. Tyszer, N. Zacharia, "Test Data Decompression for Multiple Scan Designs with Boundary Scan," <i>IEEE Transactions on Computers</i> , Vol. 47, No. 11, November 1998, pp. 1188-1200.	
		J. Rajski and J. Tyszer, "Design of Phase Shifters for BIST Applications", <i>Proc. VLSI Test Symposium</i> , pp. 218-224, 1998.	
		J. Rajski, N. Tamarapalli, J. Tyszer, "Automated Synthesis of Large Phase Shifters for Built-In Self-Test," <i>International Test Conference</i> , Paper 41.1, pp. 1047-1056, IEEE 1998	
		Venkataraman, Rajski, Hellebrand, and Tarnick, "An Efficient BIST Scheme Based on Reseeding of Multiple Polynomial Linear Feedback Shift Registers", pp. 572-577, 1993 IEEE	
		P.H. Bardell, W.H. McAnney, J. Savir, "Built in test for VLSI: Pseudorandom Techniques, John Wiley & Sons, 1987, pp. 61-88	
		W-B, Jone and S.R. Das, "Space compression method for built-in self testing of VLSI circuits," <i>Int. Journal of Computer Aided VLSI Design</i> , vol. 3, pp. 309-322, 1991.	
		H.J. Wunderlich, "On computing optimized input probabilities for random tests," <i>Proc. DAC</i> pp. 392-398, 1987.	
		N.R. Saxena and J.P. Robinson, "Accumulator compression testing," <i>IEEE Trans. Comput.</i> , vol. C-35, No. 4, pp. 317-321, 1986.	
		J.P. Hayes, "Check sum test methods," <i>Proc. FTCS</i> , pp. 114-120, 1976.	
		J. Savir, "Syndrome-testable design of combinational circuits," <i>IEEE Trans. Comput.</i> Vol. C-29, No. 6, pp. 442-451, 1980.	
		Y.K. Li and J.P. Robinson, "Space compression methods with output data modification," <i>IEEE Trans. CAD of Integrated Circuits and Systems</i> , vol. CAD-6, No. 2, pp. 290-294, 1987.	
		J.E. Smith, "Measures of the effectiveness of fault signature analysis," <i>IEEE Trans. Comput.</i> , vol. C-29, No. 6, pp. 510-514, 1980.	

EXAMINER SIGNATURE:	DATE CONSIDERED:
* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Attorney Docket Number	1011-67627
		Application Number	Not yet assigned
		Filing Date	February 17, 2004
		First Named Inventor	Rajski
		Art Unit	--
		Examiner Name	--
Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS	
		K.J. Latawiec, "New method of generation of shifted linear pseudorandom binary sequences", <i>Proc. IEE</i> , vol. 121, No. 8, pp. 905-906, 1974	
		N.R. Saxena and E.J. McCluskey, "Extended precision checksums," <i>Proc. FTCS</i> , pp. 142-147, 1987.	
		J.P. Hayes, "Transition count testing of combinational logic circuits," <i>IEEE Trans. Comput.</i> , vol. C-25, No. 6, pp. 613-620, 1976.	
		P.H. Bardell and W.H. McAnney, "Pseudorandom arrays for built-in tests," <i>ISSS Trans. Comput.</i> , vol. C-35, No. 7, pp. 653-658, 1986.	
		B. Ireland and J.E. Marshall, "Matrix method to determine shift-register connections for delayed pseudorandom binary sequences," <i>Electronics Letters</i> , vol. 4 No. 15, pp. 309-310, 1968.	
		J.A. Waicukauski, E. Lindbloom, E.B. Eichelberger, O.P. Forlenza, "A method for generating weighted random test patterns," <i>IBM J. Res. Develop.</i> , vol. 33, no. 2, pp. 149-161, March 1989	
		R.A. Frowerk, "Signature analysis: a new digital field services method," <i>Hewlett-Packard Journal</i> , pp. 2-8, May 1997.	
		G. Hetherington, T. Fryars, N. Tamarapalli, M. Kassab, A. Hasson and J. Rajski, "Logic BIST for Large Industrial Designs: Real Issues and Case Studies," <i>Proc. ITC</i> , pp. 358-367, 1999.	
		V. Iyengar, K. Chakrabarty, and B.T. Murray, "Built-In Self-testing of sequential circuits using precomputed test sets," <i>Proc. VLSI Test Symposium</i> , pp. 418-423, 1998	
		A. JAS, J. Ghosh-Dastidar, and N.A. Touba, "Scan vector compression/decompression using statistical coding," <i>Proc. VLSI Test Symposium</i> , pp. 114-120, 1999	
		A.Jas, and N.A. Touba, "Test vector decompression via cyclical scan chains and its application to testing core-based designs," <i>Proc. ITC</i> , pp.458-464, 1998.	
		H.J. Wunderlich, "Multiple distribution for biased random test patterns," <i>Proc. ITC</i> , pp. 236-244, 1988.	
EXAMINER SIGNATURE:		DATE CONSIDERED:	
* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Attorney Docket Number	1011-67627
		Application Number	Not yet assigned
		Filing Date	February 17, 2004
		First Named Inventor	Rajski
		Art Unit	--
		Examiner Name	--
Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS	
		T. Yamaguchi, M. Tilgner, M. Ishida, D.S. Ha, "An efficient method for compressing test data," <i>Proc. ITC</i> , pp. 191-199, 1997.	
		K. Chakrabarty, B.T. Murray, and J.P. Hayes. "Optimal space compaction of test responses," <i>Proc. ITC</i> , pp. 834-843, 1995.	
		K, Chakrabarty and J.P. Hayes, "Test response compaction using multiplexed parity trees," <i>IEEE Transactions CAD of Integrated Circuits and Systems</i> , vol. CAD-15, No. 11, pp. 1399-1408, 1996.	
		A. Ivanov, B. Tsuji, and Y. Zorian, "Programmable BIST sapce compactors," <i>IEEE Trans. Comput.</i> , vol. C-45, No. 12, pp. 1393-1404, 1996.	
		B. Pouya and N.A. Touba, "Synthesis of zero-aliasing elementary-tree space compactors," <i>Proc. VLSI Test Symp.</i> , pp. 70-77, 1998.	
		S.M. Reddy, K. Saluja, M. Karpovski, "A Data compression technique for built-in self-test," <i>IEEE Trans. Comput.</i> , vol. C-37, pp. 1151-1156, 1988.	
		M. Serra, T. Slater, J.C. Muzio, and D.M. Miller, "The analysis of one-dimensional linear cellular automata and their aliasing properties," <i>IEEE Trans. CAD of Integrated Circuits and Systems</i> , vol. CAD-9, No. 7, pp. 767-778, 1990.	
		T.W. Williams, W. Daehn, M. Gruetzner, and C.W. Starke, "Bounds and analysis of aliasing errors in linear-feedback shift registers," <i>IEEE Trans. CAD of Integrated Circuits and Systems</i> , vol. CAD-7, No. 1, pp. 75-83, 1988.	
		M. Ishida, D.S. Ha, T. Yamaguchi, "COMPACT: A hybrid method for compression test data," <i>Proc. VLSI Test Symposium</i> , pp. 62-69, 1998.	
		K. Kim, D.S. Ha, J.G. Tront, "On using signature registers as pseudorandon pattern generators in built-in self testing," <i>IEEE Trans. CAD of IC</i> , vol. CAD-7, No. 8, 1988, pp.919-928.	
		G. Mrugalski, J. Rajski, J. Tyszer, "Synthesis of pattern generators based on cellular automata with phase shifters," <i>Proc. Int. Test Conf.</i> , pp. 368-377, 1999.	

EXAMINER SIGNATURE:	DATE CONSIDERED:
* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Attorney Docket Number	1011-67627
		Application Number	Not yet assigned
		Filing Date	February 17, 2004
		First Named Inventor	Rajski
		Art Unit	--
		Examiner Name	--
Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS	
		R. Kapur, S. Patil, T.J. Snethen, and T.W. Williams, "Design of an efficient weighted random pattern generation system," <i>Proc. ITC.</i> , pp. 491-500, 1994.	
		F. Muradali, V.K. Agarwal, and B. Nadeau-Dostie, "A new procedure for weighted random built-in self-test," <i>Proc. ITC.</i> , pp. 600-669, 1990.	
		S. Pateras and J. Rajski "Cube contained random patterns and their application to the complete testing of synthesized multi-level circuits," <i>Proc. ITC.</i> , pp. 473-482, 1991.	
		J. Rajski, J. Tyszer, "Test responses compaction in accumulators with rotate carry adders," <i>IEEE Transactions CAD of Integrated Circuits and Systems</i> , vol. CAD-12, No. 4, pp. 531-539, 1993.	
		J. Rajski, J. Tyszer, "Accumulator-based compaction of test responses," <i>IEEE Transactions on Comput.</i> , vol. C-42, No. 6, pp. 643-650, 1993.	
		N.R. Saxena and E.J. McCluskey, "Analysis of checksums, extended-precision checksums, and cyclic redundancy," <i>IEEE Trans. Comput.</i> , vol. C-39, No. 7, pp. 969-975, 1990.	
		N.A. Touba and E.J. McCluskey, "Transformed pseudo-random patterns for BIST," <i>Proc. VLSI Test Symposium</i> , pp. 410-416, 1995.	
		N.A. Touba and E.J. McCluskey, "Altering a pseudo-random bit sequence for scan-based BIST," <i>Proc. ITC.</i> , pp. 167-175, 1996.	
		K.H. Tsai, S. Hellebrand, J. Rajski, and Marek-Sadowska, "STARBIST: Scan autocorrelated random pattern generation," <i>Proc. DAC</i> , pp. 472-477, 1997.	
		H.J. Wunderlich and G. Kiefer, "Bit-flipping BIST," <i>Proc. ICCAD</i> , pp. 337-343, 1996.	
		S.W. Golomb, <i>Shift Register Sequences</i> , Holden Day, San Francisco, 1967, pp. 7-22 and 75-89	
		V.N. Yarmolik and S.N. Demidenko, "Generation and Application of Pseudorandom Sequences for Random Testing, J. Wiley & Sons, New York, 1988, pp. 63-94	

EXAMINER SIGNATURE:	DATE CONSIDERED:
* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.	